The "marked-up" version of the amended claims are provided in the APPENDIX attached hereafter.

REMARKS

In response to the Office Action dated December 5, 2001, claims 1 and 2 have been amended. Claims 1-17 are now active in this application. Based on the above amendment and the following Remarks, Applicant respectfully requests that the Examiner reconsider the outstanding rejections and they be withdrawn.

Claim Rejection Under 35 U.S.C. §112

In the Office Action, claim 2 has been rejected under 35 U.S.C. §112, second paragraph for being indefinite. Particularly, the Examiner pointed out that Fig. 2 and the specification does not show "the second signal wire is connected to a ground through a predetermined resistance value" as recited in claim 2. This rejection is respectfully traversed.

Fig. 2 of the present application shows a timing controller 550 generating two clock signals CLK1 and CLK2. As shown therein, two clock signal wires are used to transfer the clock signals CLK1 and CLK2: one for transmitting the clock signal CLK1 and another for transmitting the clock signal CLK2. Particularly, the wire used for transmitting the clock signal CLK2 is connected to a ground through a predetermined resistance value Re.

Thus, Fig. 2 clearly shows "the second signal wire is connected to a ground through a predetermined resistance value". Accordingly, Applicant respectfully submits that the rejection of claim 2 under 35 U.S.C. §112, second paragraph is not viable, and hence solicit withdrawal thereof.

Claim Rejection Under 35 U.S.C. §102

In the Office Action, claims 1, 3, 4, 7, 8, 10 and 12-17 have been rejected under 35 U.S.C. §102(e)(b) for being anticipated by U. S. Patent No. 5,889,504 issued to Kihara, et al. ("Kihara"). This rejection is respectfully traversed.

With respect to independent claim 1, this claim has been amended for clarification. Claim 1 now recites "a second signal wire through which a first clock signal having a frequency equal to the shift clock signal but having a phase difference of 90° to 270° is transmitted to a ground". For example, this feature is shown in Fig. 2 and its corresponding portion of the specification. Particularly, as previously mentioned, Fig. 2 shows "the second shift clock signal CLK2, which has the same frequency as the first shift clock signal CLK1 but has an opposite phase is sent to a ground GND via a resistor Re to minimize EMI caused by the transmission of the first shift clock signal CLK1" (Page 10, lines 13-16).

In this regard, according to Kihara, a timing controller 106 sent clock signals CK and /CK to a shift register 5 of a data driver 3 to perform a shift operation of the data signal. Thus, the clock signal /CK in Kihana is sent to the data driver, not to a ground, as recited in claim 1. Accordingly, it is respectfully submitted that Kihana fails to teach the claimed feature of "a second signal wire through which a first clock signal having a frequency equal to the shift clock signal but having a phase difference of 90° to 270° is transmitted to a ground"

Regarding independent claim 10, this claim recites:

> "a timing controller for generating a first image data signal and a second image data signal and generating a first shift clock signal and a second shift clock signal with a phase difference of 90° to 270° that respectively shift the first image data signal and the second image data signal, a first image data signal wire and a second image data signal wire though which the first image data

> signal and the second image data signal are respectively transmitted, and a first shift clock signal wire and a second shift clock signal wire through which the first shift clock signal and the second shift clock signal are respectively transmitted"

Thus, according to claim 10, the timing controller generates (a) the first image data signal (b) the second image data signal, (c) the first shift clock signal, and (d) the second shift clock signal. The first and second shift clock signals respectively shift the first and second image data signal. Also, there are four wires, which are (a) the first image data signal wire, (b) the second image data signal wire, (c) the first shift clock signal wire, and (d) the second shift clock signal wire. The first and second image data signals are respectively transmitted through the first and second image data signal wires, and the first and second shift clock signals are respectively transferred through the first and second shift clock signal wires. For example, Fig. 6 shows a timing controller 750 generating two image data signals (even and odd image data signals) and two shift clock signals CLK3 and CLK4.

In the Office Action, the Examiner asserted that this claimed feature is described in column 5, lines 29-44 of Kihara, which reads:

> "The data driver 3 has a sampling transistor circuit 4 and a shift register 5 which controls the operation of the sampling transistor circuit 4. The shift register circuit 5 receives a clock signal CK and /CK, and the data signal in accordance with the clock signal provided by an external timing controller 106. The shift register circuit 5 then performs a shift operation of the data signal in accordance with the clock signal CK and /CK. The shift register circuit 5 further controls the sampling transistor circuit 4 in order that the video signal provided by an external video signal processing circuit 103 via a video line VL can be applied to each of the data lines $D_1 \ldots D_{16m}$. A shift selection circuit 6 sets the direction of the shifting to the left or right in accordance with the specifications of the LCD, then outputs a shift direction signal DR, which indicates the set direction, to the shift register circuit 5"

Thus, Kihara states that the data signal is provided by the external timing controller 106. However, Kihara fails to teach or suggest the external timing controller 106 generating two separate data signals, as claimed. Also, Kihara is silent as to two separate image data signal wires which transmit the two separate data signals, respectively. Rather, according to Kihara, the external video signal processing circuit 103 generates a video signal which is applied to each of the data lines $D_1 \ldots D_{16m}$. Thus, according to Kihara, the timing controller 106 does not generate "a first image data signal and a second image data signal". Thus, it would not be possible for Kihara to teach "a first image data signal wire and a second image data signal wire though which the first image data signal and the second image data signal are respectively transmitted".

Accordingly, Applicants respectfully submit that the rejection of independent claims 1 and 10 and their dependent claims , 3, 4, 7, 8 and 12-17 under 35 U.S.C. §102(e) by Kihara is not viable, and hence solicit withdrawal thereof.

Claim Rejection Under 35 U.S.C. §103

In the Office Action, claims 5, 6, 9 an 11 have been rejected under 35 U.S.C. §103(a) for being unpatentable over Kihara. This rejection is respectfully traversed.

Claims 5, 6, 9 stem from claim 1 and claim 11 stems from claim 10. As previously mentioned, the independent claims 1 and 10 are patentably distinguishable from Kihara. No secondary reference has been introduced to cure the deficiency from the teachings of Kihara. Thus, it would not have been obvious to modify the teachings of Kihara to arrive at the claimed invention.

Accordingly, Applicants respectfully submit that the rejection of claims 5, 6, 9 and 11 under 35 U.S.C. §103(a) over Kihara is not viable/has been overcome, and hence solicit withdrawal thereof.

CONCLUSION

All of the stated grounds of objection and rejection have been properly traversed, accommodated, or rendered moot. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete response has been made to the outstanding Office Action and, as such, claims 1-17 are in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment is respectfully requested.

Respectfully submitted,

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APPENDIX

The "marked-up" version of the amended claims is as follows:

1. (Amended) A liquid crystal display system comprising:

a liquid crystal display panel including a plurality of data lines, a plurality of gate lines intersecting the data lines, and a plurality of pixel electrodes arranged in a matrix type and each having a switch connected to one of the gate lines and one of the data lines;

a gate driver for successively applying a gate voltage to the gate lines to turn on the switches;

a data driver for applying a gray voltage, corresponding to image data signals, to the data lines; [and]

a timing controller for sending [both] the image data signals and a shift clock signal to the data driver, [with]

a first signal wire through which the shift clock signal is transmitted to said data driver[,]; and

a second signal wire through which a first clock signal having a frequency equal to the shift clock signal but having a phase difference of 90° to 270° is transmitted to a ground.

2. (Amended) The liquid crystal display system of claim 1 wherein the second signal wire is connected to [a] said ground through a predetermined resistance value.